

using said second synchronous sequence as a basis for said simulation testing of said design.

1 2. A method of generating a synchronous sequence of test vectors from
2 information originating within an asynchronous environment comprising:
3 providing a simulation synchronous sequence of states,
4 wherein each of said states is referenced to a clock period, said simulation
5 synchronous sequence being partially based on event timing parameters of
6 a particular system of interest;
7 introducing short timing delays to said states within specific said
8 clock periods of said simulation synchronous sequence to generate an
9 asynchronous short-delay sequence of states, durations of specific said short
10 timing delays being responsive to event timing parameters of a particular
11 integrated circuit (IC) design;
12 comparing said states of said asynchronous short-delay
13 sequence, including correlating a plurality of said clock periods having said
14 states of said asynchronous short-delay sequence to identify a first over-
15 lapping time interval, said first overlapping time interval being consistent with
16 a time coincidence among said states of said asynchronous short-delay
17 sequence;
18 introducing long timing delays to said states within specific
19 said clock periods of said simulation synchronous sequence to generate
20 an asynchronous long-delay sequence of states, durations of specific said
21 long timing delays being responsive to event timing parameters of said
22 particular IC;
23 comparing said states of said asynchronous long-delay
24 sequence, including correlating a plurality of said clock periods having said
25 states of said asynchronous long-delay sequence to identify a second
26 overlapping time interval, said second overlapping time interval being
27 consistent with a time coincidence among said states of said asynchronous
28 long-delay sequence;
29 generating a synchronous long-delay sequence by successively
30 repeating a second delay-adjusted clock period having a state which is
31 delayed by said second overlapping time interval; and
32 comparing said synchronous short-delay sequence with timing
33 of said states of said synchronous long-delay sequence to generate said
34 synchronous sequence of test vectors, including time aligning said
35 synchronous short-delay and long-delay sequences to detect a plurality of
36 overlapping sampling time intervals for locating said synchronous sequence
37 of test vectors.

1 3. The method of claim 2 wherein said step of introducing said short timing
2 delays includes adding best case tester-load timing delays to said clock
3 periods of said simulation synchronous sequence, said best case tester-load
4 timing delays being indicative timing constraints of an IC tester.

1 4. The method of claim 2 wherein said step of introducing said short timing
2 delays includes adding best case chip-load timing delays indicative of timing
3 constraints of said IC design.

1 5. The method of claim 3 wherein said step of introducing said long timing
2 delays includes adding worst case tester-load timing delays that are indicative
3 of said timing constraints of said IC tester.

1 6. The method of claim 4 wherein said step of introducing said long timing
2 delays includes adding worst case chip-load timing delays indicative of said
3 timing constraints of said IC.

1 7. The method of claim 2 wherein said step of providing said simulation
2 synchronous sequence includes:
3 providing a simulated asynchronous sequence of states;
4 extracting a state of said asynchronous sequence at each said
5 clock period to generate a simulated synchronous sequence of states;
6 introducing an abbreviated timing delay to each said clock
7 period of said simulated synchronous sequence to generate a simulated
8 synchronous abbreviated-delay sequence and introducing an extended timing
9 delay to each said clock period of said simulated synchronous sequence to
10 generate a simulated synchronous extended-delay sequence; and
11 comparing said simulated synchronous abbreviated-delay
12 sequence to said simulated synchronous extended-delay sequence, including
13 time aligning said simulated synchronous abbreviated-delay and extended-
14 delay sequences to detect a plurality of overlapping second time intervals
15 for defining positions of states in said clock periods of said simulation
16 synchronous sequence.

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1 8. The method of claim 7 wherein said step of introducing said abbreviated
2 timing delay and said extended timing delay includes executing said
3 simulated synchronous sequence under respective best case timing delay
4 and worst case timing delay scenarios in a system simulation environment,
5 said system simulation environment having timing characteristics indicative of
6 said particular system of interest.

1 9. The method of claim 7 further including adapting said simulated
2 synchronous extended-delay sequence as said simulation synchronous
3 sequence when there is not an acceptable number of said overlapping
4 second time intervals.

1 10. The method of claim 7 wherein said step of providing said simulated
2 asynchronous sequence includes selecting said clock period to have a
3 duration that corresponds to a tester clock period of an IC tester.

1 11. The method of claim 2 further including selectively fixing a sampling
2 instance in one of said overlapping sampling time intervals to correspond to a
3 rising edge of a tester clock period of an IC tester.

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1 12. A test vector generator for generating a synchronous sequence of test
2 vectors comprising:

3 a simulation module that is enabled to generate a simulation
4 synchronous sequence of states under a system simulation environment, said
5 simulation synchronous sequence including a plurality of timing regions for
6 identifying operations of an integrated circuit (IC) design;

7 a delay module that is enabled to introduce short delays and
8 long delays to said simulation synchronous sequence to respectively generate
9 asynchronous short-delay sequence and asynchronous long-delay sequence,
10 each of said short delays and said long delays being timing delays associated
11 with at least one of an integrated circuit (IC) and an IC tester;

12 an overlaying module that is configured to provide a first state
13 overlapping time interval and a second state overlapping time interval by
14 respectively comparing a plurality of base periods of said asynchronous
15 short-delay sequence and comparing a plurality of base periods of said
16 asynchronous long-delay sequence;

17 a duplication module that is configured to incorporate said first
18 state time interval into a first sequence of said base periods and to incorpo-
19 rate said second state overlapping time interval into a second sequence of
20 said base periods to respectively generate a synchronous short-delay
21 sequence and a synchronous long-delay sequence; and

22 a sequence overlaying module that is configured to time align
23 said synchronous short-delay sequence and said synchronous long-delay
24 sequence to detect a plurality of overlapping sampling intervals for locating
25 said synchronous sequence of test vectors.

1 13. The test vector generator of claim 12 wherein said short delays are
2 related to a best case chip-load timing delay of said IC and a best case tester-
3 load timing delay of said IC tester.

1 14. The test vector generator of claim 13 wherein said long delays are
2 related to a worst case chip-load timing delay of said IC and a worst case
3 tester-load timing delay of said IC tester.

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1 15. The test vectors generator of claim 12 further comprising a verification
2 module that is configured to execute said synchronous sequence of test
3 vectors under said short delays and said long delays for verifying timing
4 correctness.

1 16. The test vectors generator of claim 12 wherein said system simulation
2 environment is independent of any delay associated with said IC and said IC
3 tester.

1 17. The test vectors generator of claim 12 wherein said base period is a time
2 interval that is equivalent to a tester period of said IC tester.

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1 18. A method for converting asynchronous states into synchronous states to
2 generate a synchronous sequence of test vectors for verifying functionality of
3 a simulated integrated circuit (IC) design comprising:

4 providing a simulation synchronous sequence of states;
5 generating an asynchronous short-delay sequence of first
6 periods and an asynchronous long-delay sequence of second periods,
7 including inserting short delays and long delays into said simulation
8 synchronous sequence, said short delays and said long delays characterizing
9 timing delays of at least one of said simulated IC and a tester;

10 detecting a short-delay overlapping time interval and a long-
11 delay overlapping time interval, including correlating a plurality of said first
12 periods to identify said short-delay overlapping time interval and correlating a
13 plurality of said second periods to identify said long-delay overlapping time
14 interval;

15 generating a synchronous short-delay sequence of states by
16 forming a succession of substantially identical base periods that include a
17 state and said short-delay overlapping time interval;

18 generating a synchronous long-delay sequence of states by
19 forming a succession of substantially identical base periods that include a
20 state and said long-delay overlapping time interval; and

21 generating said synchronous sequence of test vectors, including
22 time-aligning said synchronous short-delay sequence and said synchronous
23 long-delay sequence and identifying overlapping timing envelopes of states
24 within corresponding said base periods of said synchronous short-delay and
25 long-delay sequences.

1 19. The method of claim 18 wherein said step of inserting said short delays
2 and said long delays includes respectively introducing best-case timing delays
3 of said IC and worst-case timing delays of said IC.

1 20. The method of claim 19 wherein said step of inserting said short delays
2 and said long delays includes respectively introducing best-case timing delays
3 of said tester and worst-case timing delays of said tester.